REMARKS

Introduction

Claims 1-37 were pending in this application.

Claims 1-15 and 17-36 have been allowed.

Claims 16 and 37 have been rejected under 35 U.S.C. § 112, ¶ 1, as failing to comply with the enablement requirement.

Applicant has amended claims 16 and 37 to more clearly define the claimed invention. No new matter has been added and the amendments are fully supported by the originally-filed specification.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Claims 1-15 and 17-36

Applicant thanks the Examiner for indicating the allowance of claims 1-15 and 17-36.

Claims 16 and 37

The Examiner has rejected claims 16 and 37 under 35 U.S.C. § 112, ¶ 1, as failing to comply with the enablement requirement. In particular, the Examiner states that in claims 16 and 37:

> "*said first and second signals are said first and second output signals*", lines 10-12, appears to be not supported by the disclosure since *the first and second output signals* are derived from *the first and second signals* and

> there is no feedback relationship between *the first and second output signals* and *the first and second signals*.

(Office Action, p. 2, ¶ 2). These rejections are respectfully traversed.

Applicant has amended claims 16 and 37 to more clearly define the claimed invention. Applicant's claims 16 and 37 are directed to a method and apparatus for signal delay adjustment. In step a), a first output signal is generated having a first phase between the phases of first and second input signals. In step b), a second output signal is generated having a second phase not equal to the first phase between the phases of the first and second input signals. In step c), steps a) and b) are repeated a predetermined number of times such that (1) the first output signal generated from a preceding step a) becomes the first input signal in subsequent steps a) and b), and (2) the second output signal generated from a preceding step b) becomes the second input signal in the subsequent steps a) and b) (emphasis added). In step d), a final output signal is generated having a phase between the first phase of the first output signal and the second phase of the second output signal generated from step c) after the predetermined number of times.

Contrary to the Examiner's contention, support for claims 16 and 37 can be found in FIGS. 6-7 and on page 15, line 17 through page 19, line 25 of the specification. FIG. 6 shows a phase mixer block having multiple stages of cascaded

phase mixers. For example, two input signals 602/604 are sent as input to a first mixing stage 620 where two output signals 624/628 are generated, each having phases between the phases of the two input signals 602/604 (i.e., steps a and b of claims 16 and 37). The output signals 624/628 from the first mixing stage 620 are then sent as input to a second mixing stage 630 where another two output signals 634/638 are generated, each having phases between the phases of the input signals 624/628 (i.e., step c of claims 16 and 37). The output signals 654/658 from a second-to-last mixing stage 650 are then sent as input to a last mixing stage 660 where a final output signal 664 is generated having a phase between the phases of the input signals 654/658 (i.e., step d of claims 16 and 37). (Applicant's specification, FIG. 6; p. 15, line 17 to p. 17, line 25).

As described in claims 16 and 37 and supported by the specification, at each mixing stage, output signals are generated having phases between the phases of the input signals to that mixing stage. The output signals generated by a preceding mixing stage are used as input to a subsequent mixing stage in order to generate further output signals. Thus, contrary to the Examiner's contentions, no feedback relationship is necessary for the first and second output signals to be derived from the first and second input signals, and for the first and second output signals generated from

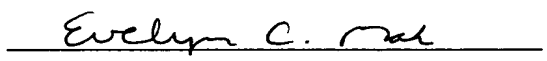
preceding steps a) and b) to be first and second input signals in subsequent steps a) and b) as recited in claims 16 and 17.

For at least the foregoing reasons, applicant respectfully submits that claims 16 and 37, as amended, comply with the enablement requirement and are in condition for allowance.

Conclusion

Applicant respectfully submits that this application, including claims 1-37, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,



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